2024
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

A UVM Testbench for Checking the Global Convergence of Analog/Mixed-Signal Systems: An Adaptive Decision Feedback Equalizer Example

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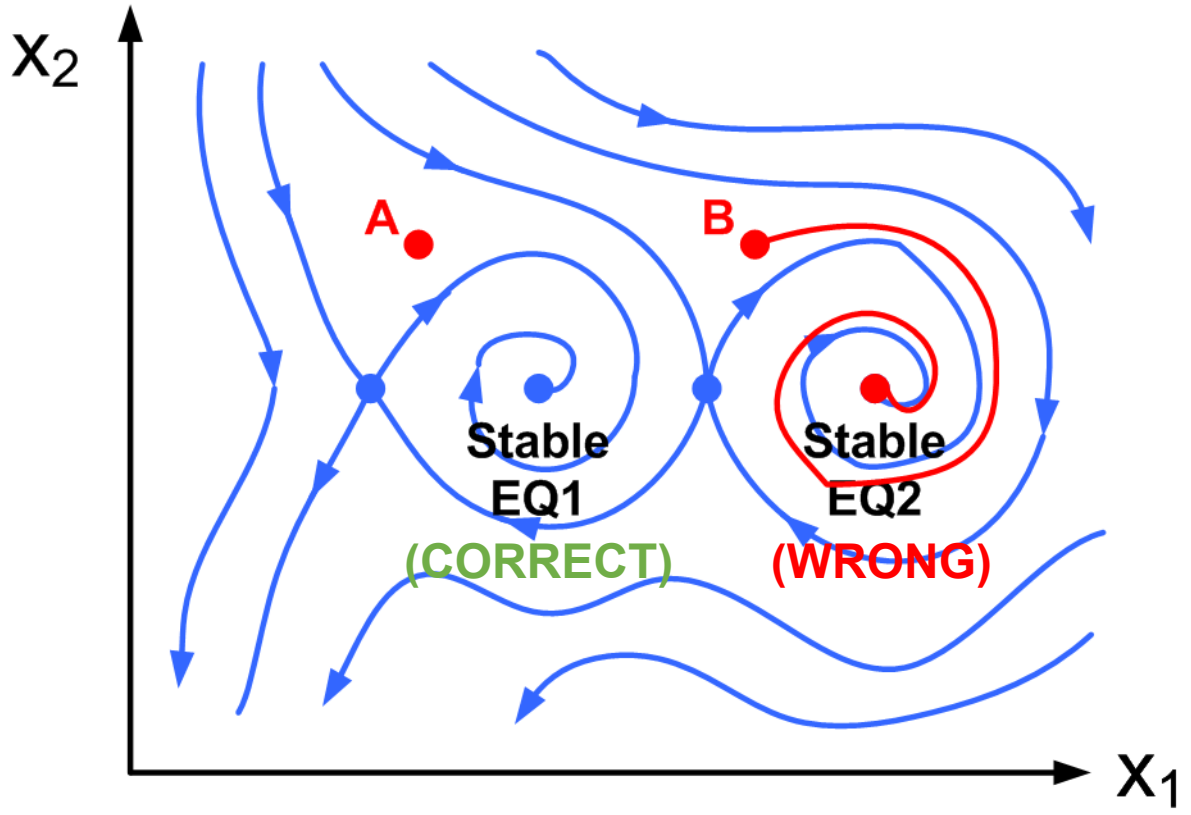
SYSTEMS INITIATIVE

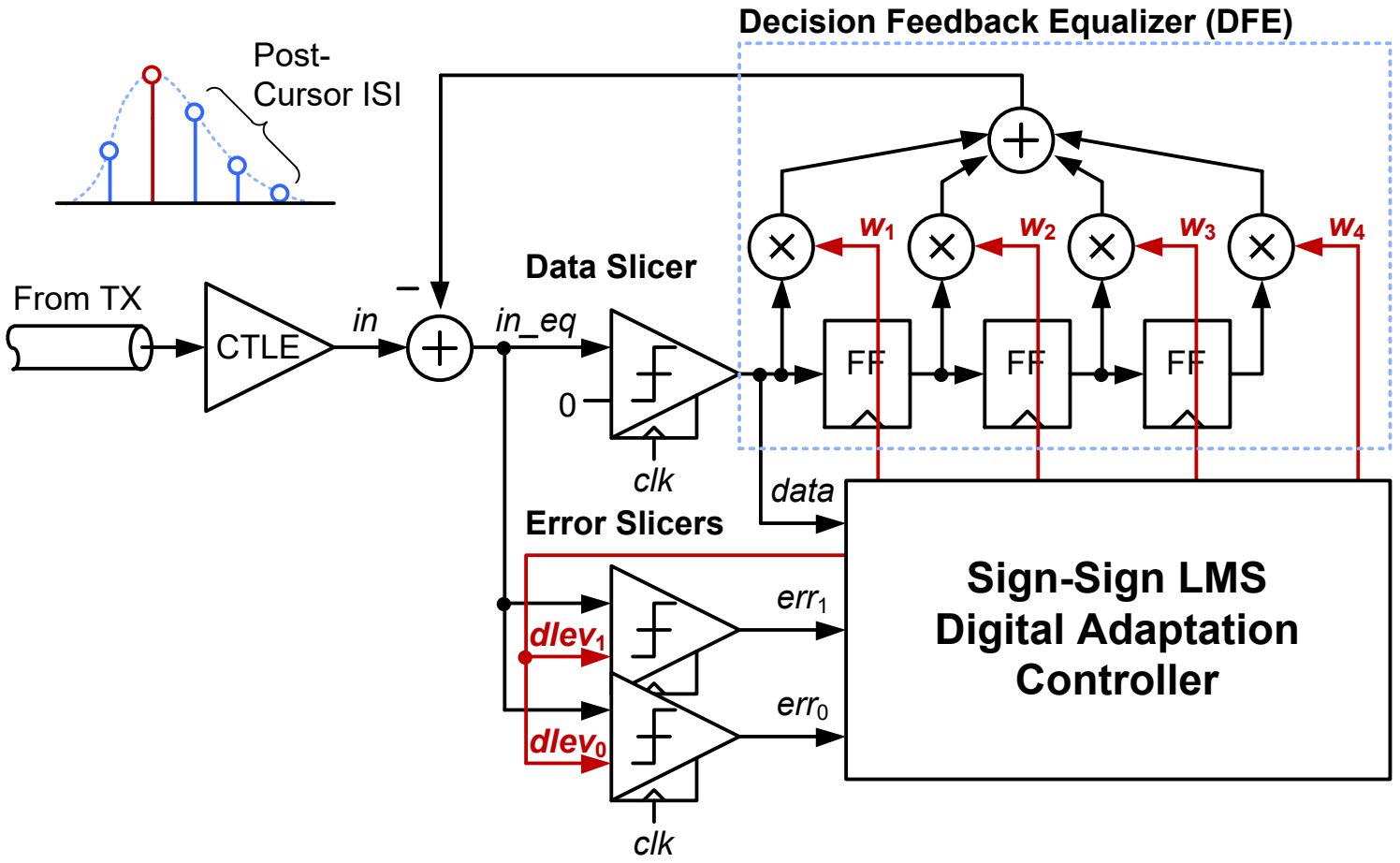
Global Convergence Failures in AMS Systems

- A nonlinear system may settle to a different final state depending on the initial state
  - Due to the existence of multiple stable equilibrium states
- Many digital calibration loops for analog circuits are prone to this kind of failures
  - Due to the nonlinearities introduced by the digital controllers



Adaptive Decision-Feedback Equalizer (DFE)

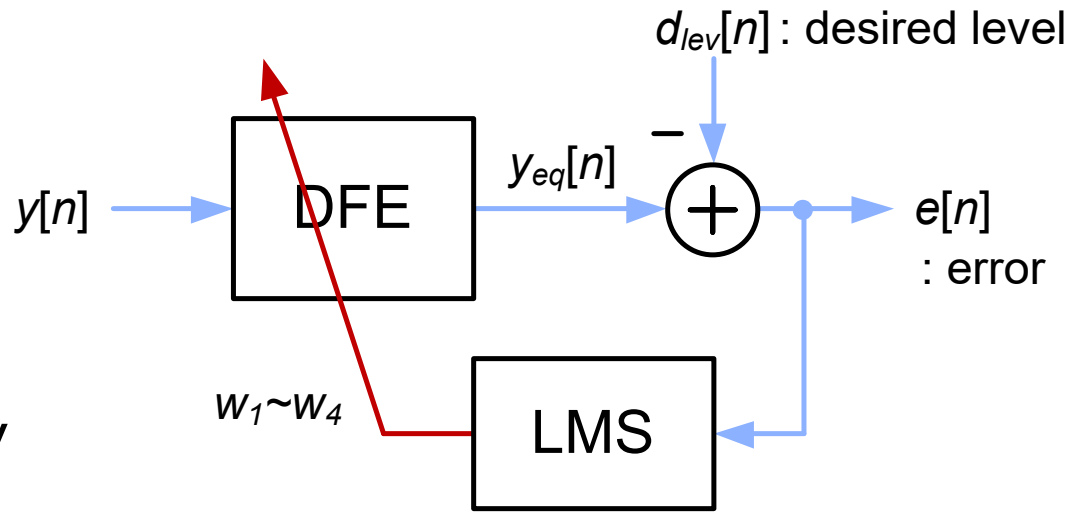
- DFE reconstructs the post-cursor ISI caused by the previous bits using a FIR filter and subtracts it from the input
- A digital adaptation loop adjusts the filter weights (w_1~w_4) based on the data and error polarities (*data*, err_0 & err_1)



Sign-Sign LMS Adaptation Algorithm

- Least mean squares (LMS) algorithm adjusts w_1~w_4 to reduce the error $e[n]$:

$$\Delta w_k = -\frac{\mu}{2} \cdot \frac{\partial e^2[n]}{\partial w_k} = -\mu \cdot e[n] \cdot y[n-k]$$



- Sign-sign LMS algorithm approximately computes the polarity of Δw_k:

$$\Delta w_k = -\mu \cdot sign(e[n]) \cdot sign(y[n-k])$$
$$\approx -\mu \cdot \boxed{sign(e[n])} \cdot \boxed{sign(y_{eq}[n-k])}$$

$= err_0$ & err_1 $\quad$ $= data$

It is this approximation ($y \approx y_{eq}$) that causes global convergence issues! (e.g. when w_1~w_4 are large)

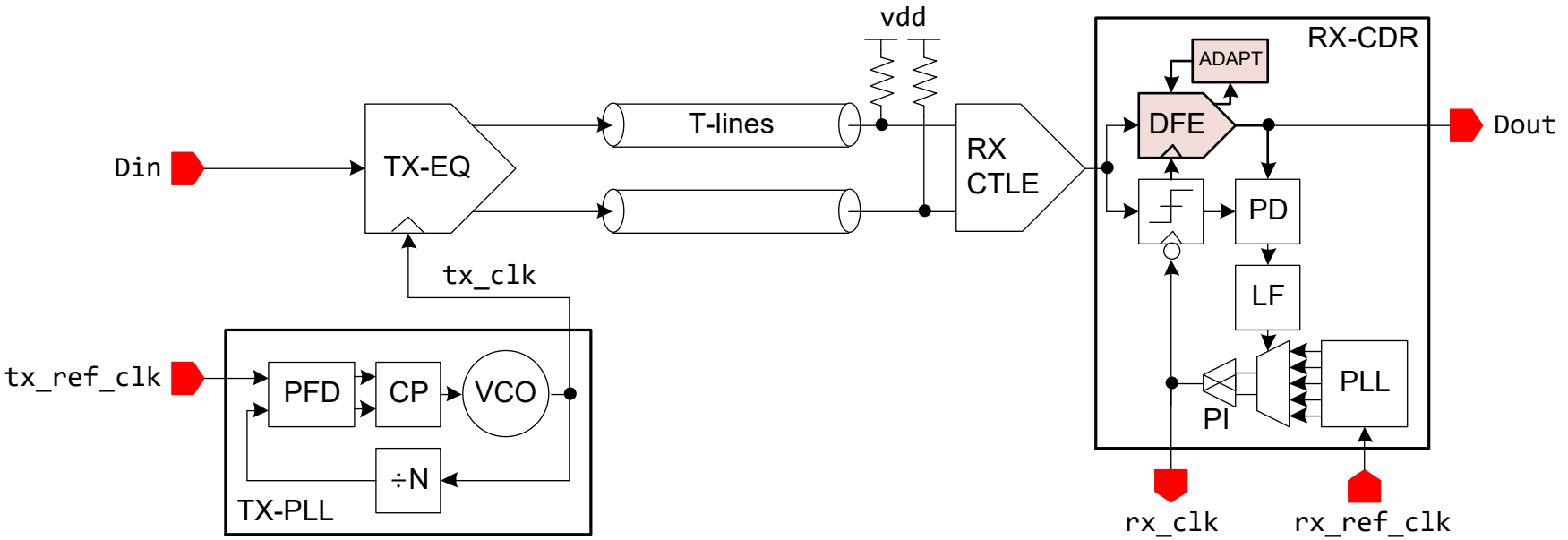
Goal of This Work

- Build a UVM testbench that can check the global convergence property of a sign-sign LMS adaptation loop for DFE
  - Does the loop always converge to the same state regardless of the initial state?

- To achieve this, we need to:
  - Model the wireline receiver including DFE in SystemVerilog; and
  - Test all possible initial states and check their convergence to the same final state

Modeling a High-Speed Wireline Transceiver

- Requires capabilities of simulating ***analog*** signals driven by a transmitter, propagating through a lossy channel, and equalized & detected by a receiver along with a ***digital*** adaptation loop in ***SystemVerilog***

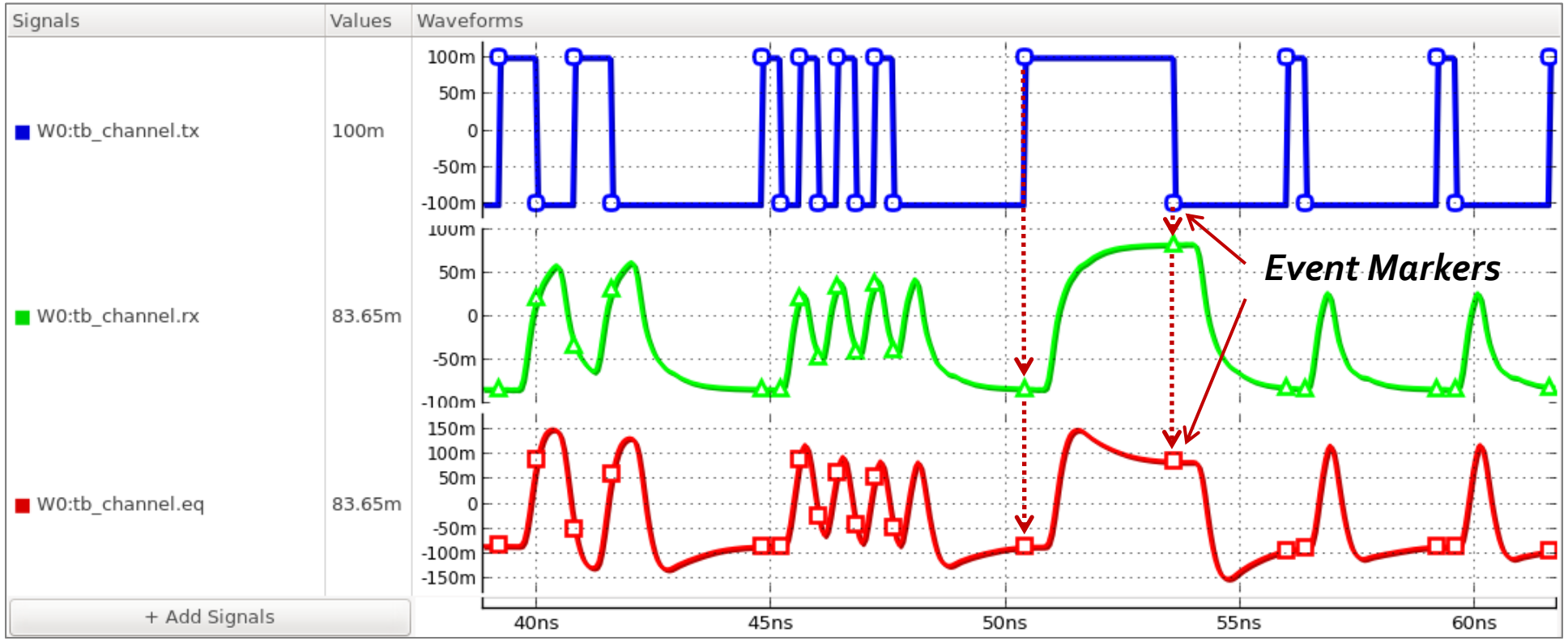


XMODEL Enables Analog in SystemVerilog/UVM

- *XMODEL* is a plug-in extension enabling ***fast and accurate analog/mixed-signal*** simulation in ***SystemVerilog***
  - ***Event-driven***: delivering 10~100x faster speed than Real-Number Model (RNM)
  - ***Analog***: supporting both functional and circuit-level models
  - ***SystemVerilog***: fully compliant with SystemVerilog-based flows (e.g. UVM)

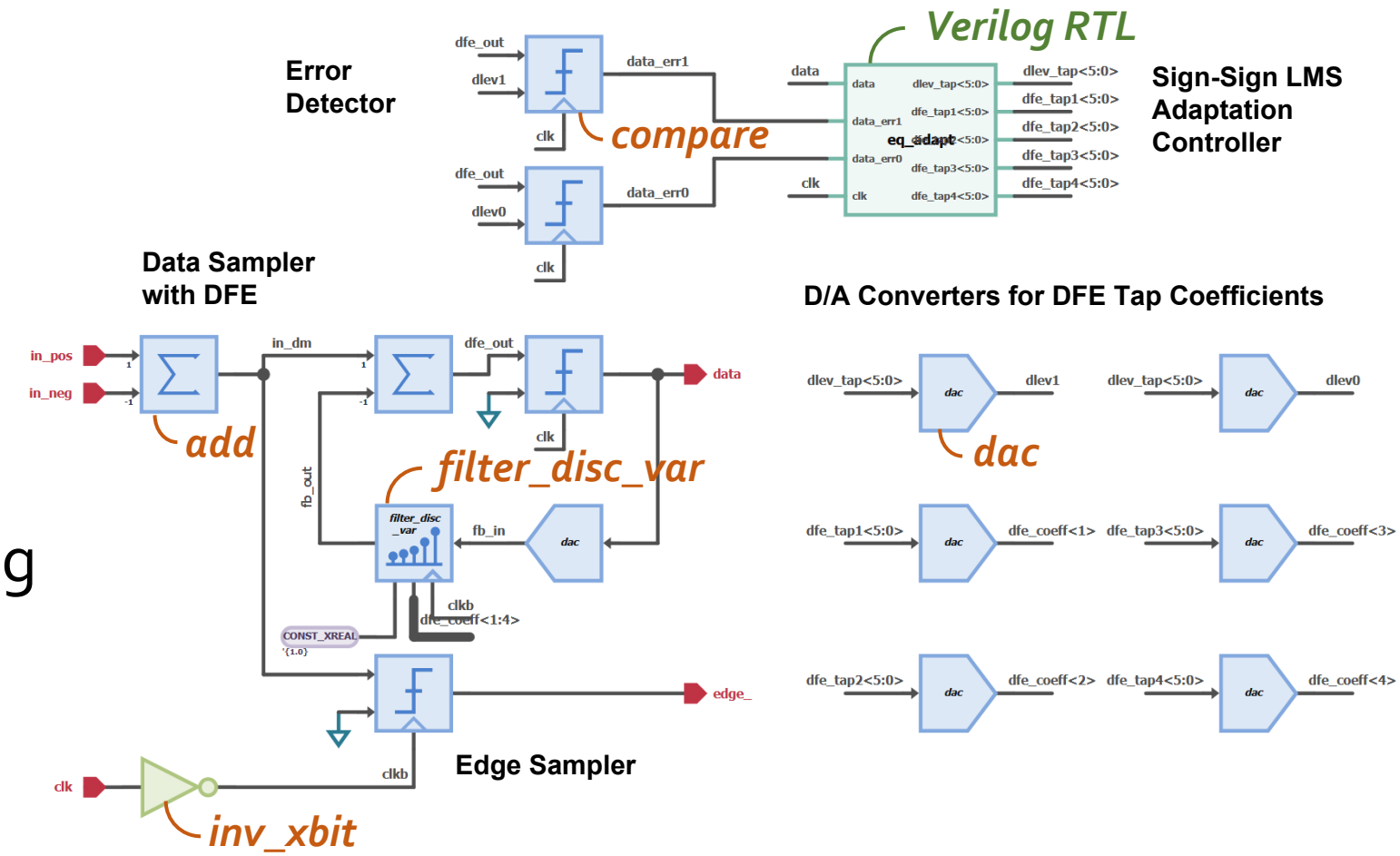
Event-Driven Simulation of *XMODEL*

- Ideal for simulating data pulses through the lossy channel and equalizer



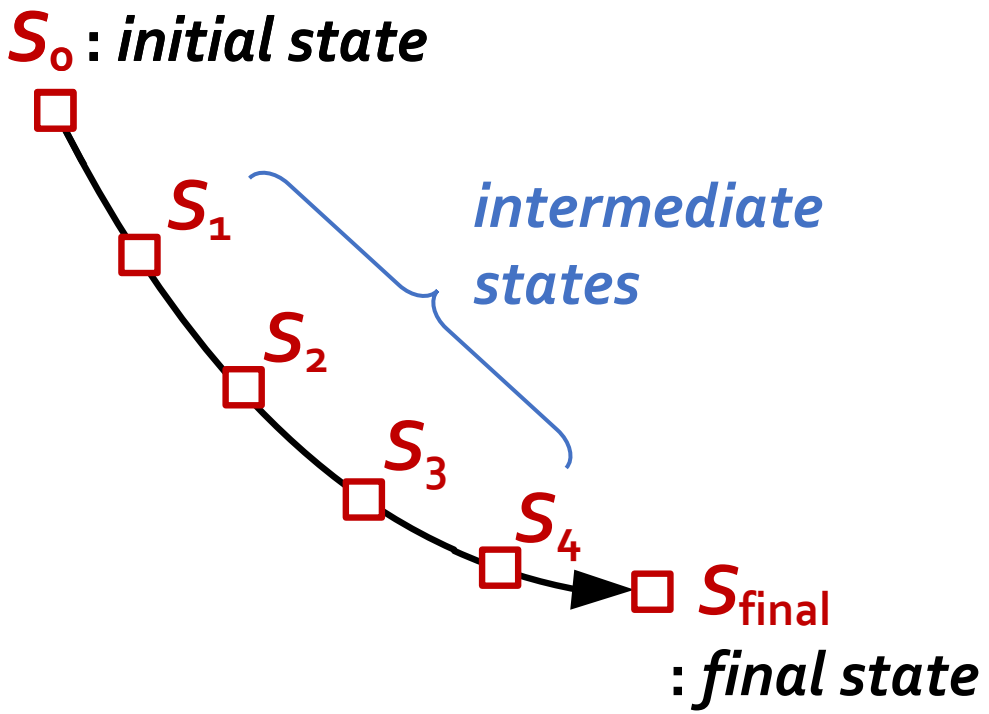
Modeling a DFE Receiver with *XMODEL*

- Analog circuits are modeled using *XMODEL* primitives as building blocks
- Digital blocks are modeled in SystemVerilog



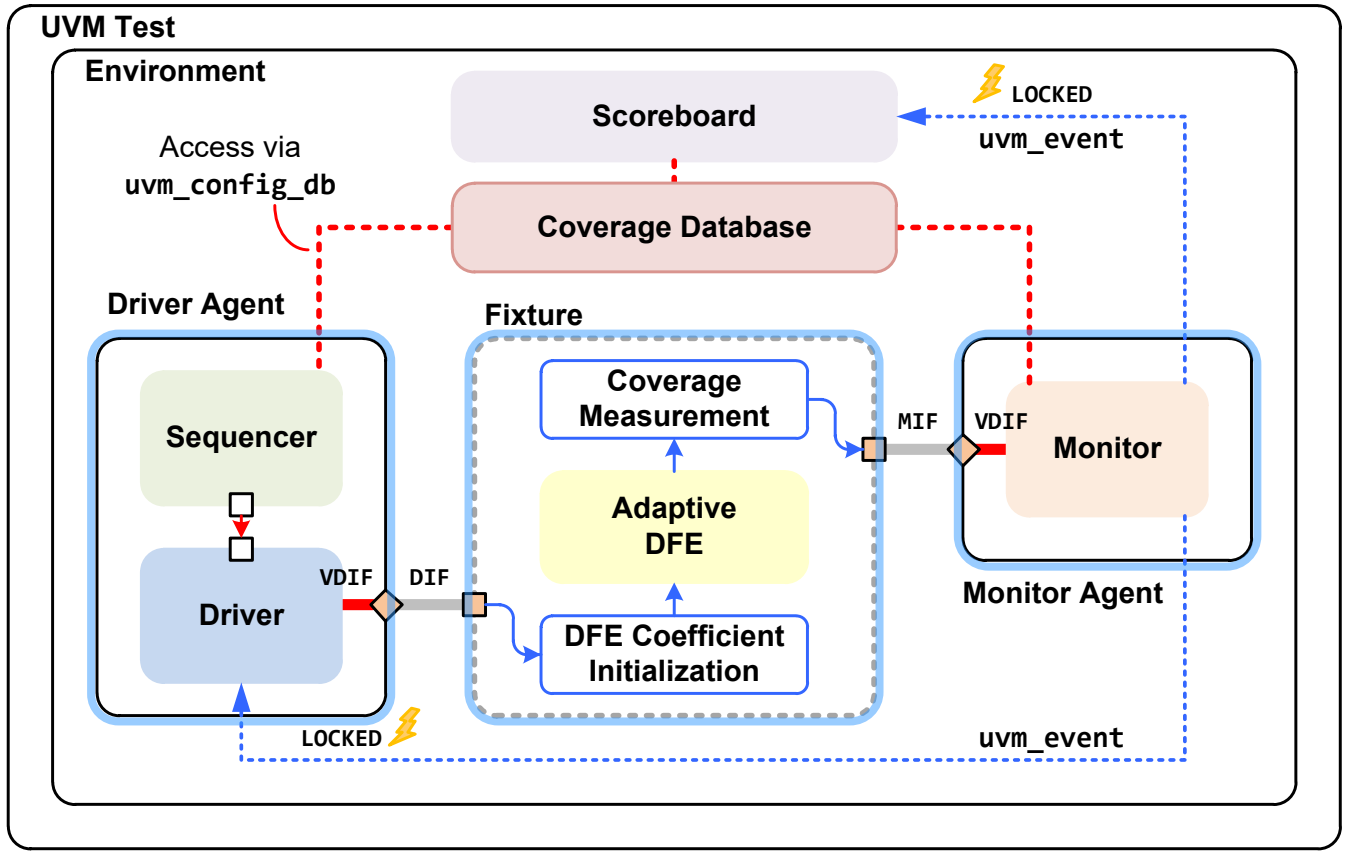
Verifying Global Convergence

- Adaptation controller incrementally adjusts the DFE weights w_1~w_4
  - State := digital values of w_1~w_4
- We want to check if all initial states eventually lead to the same final state
  - Each trial with an initial state (S_0) may pass through some intermediate states (S_1~S_4) before reaching the final state (S_{final})
  - S_0~S_4 are verified as the initial states that converge to S_{final} → ***Save # of trials required!***



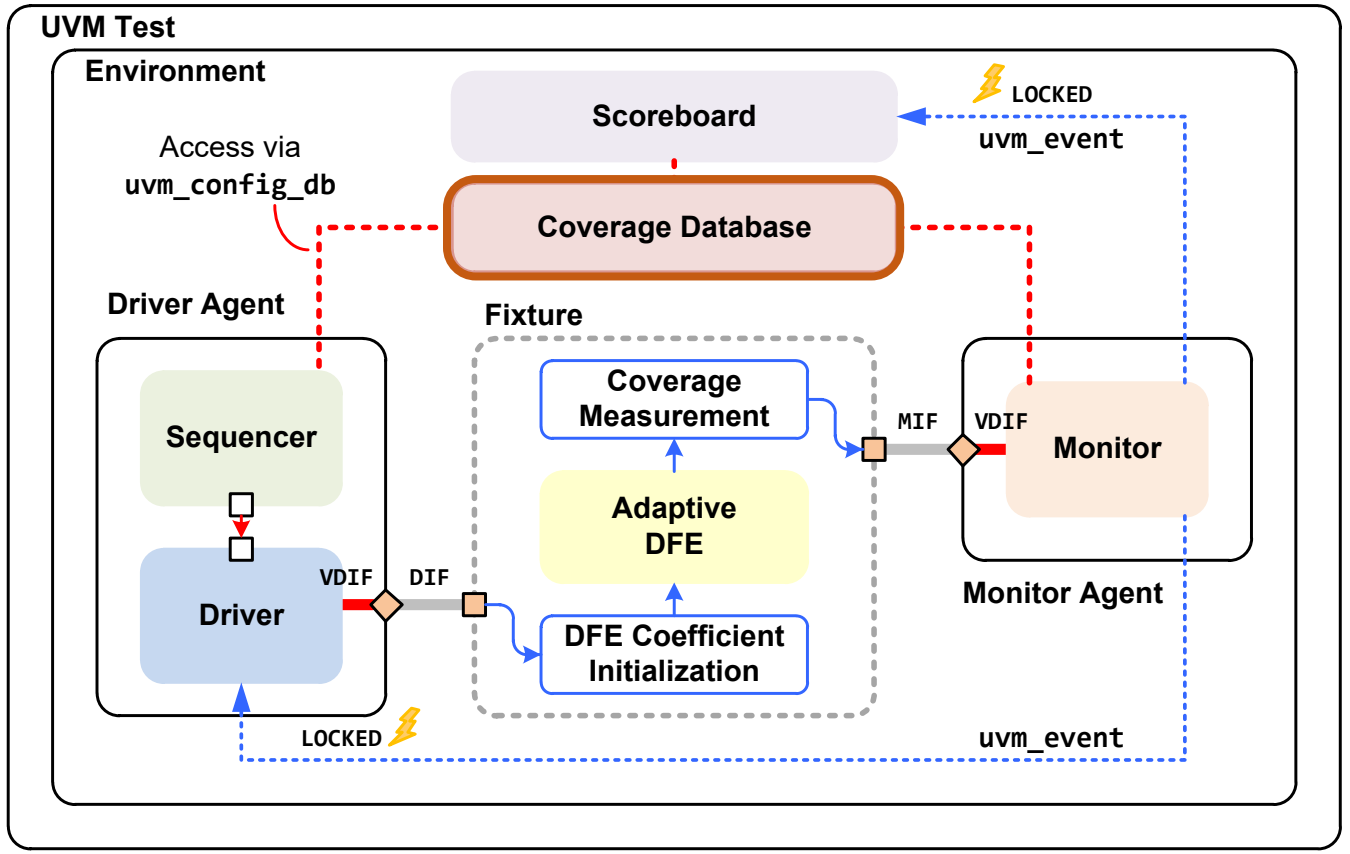
UVM Testbench for Verifying Global Convergence

- ***Driver agent*** selects an unexplored state to start a new trial with
- ***Fixture module*** initializes the DUT's state and collect its traversals
- ***Monitor agent*** detects whether a final state or a previously explored state is reached



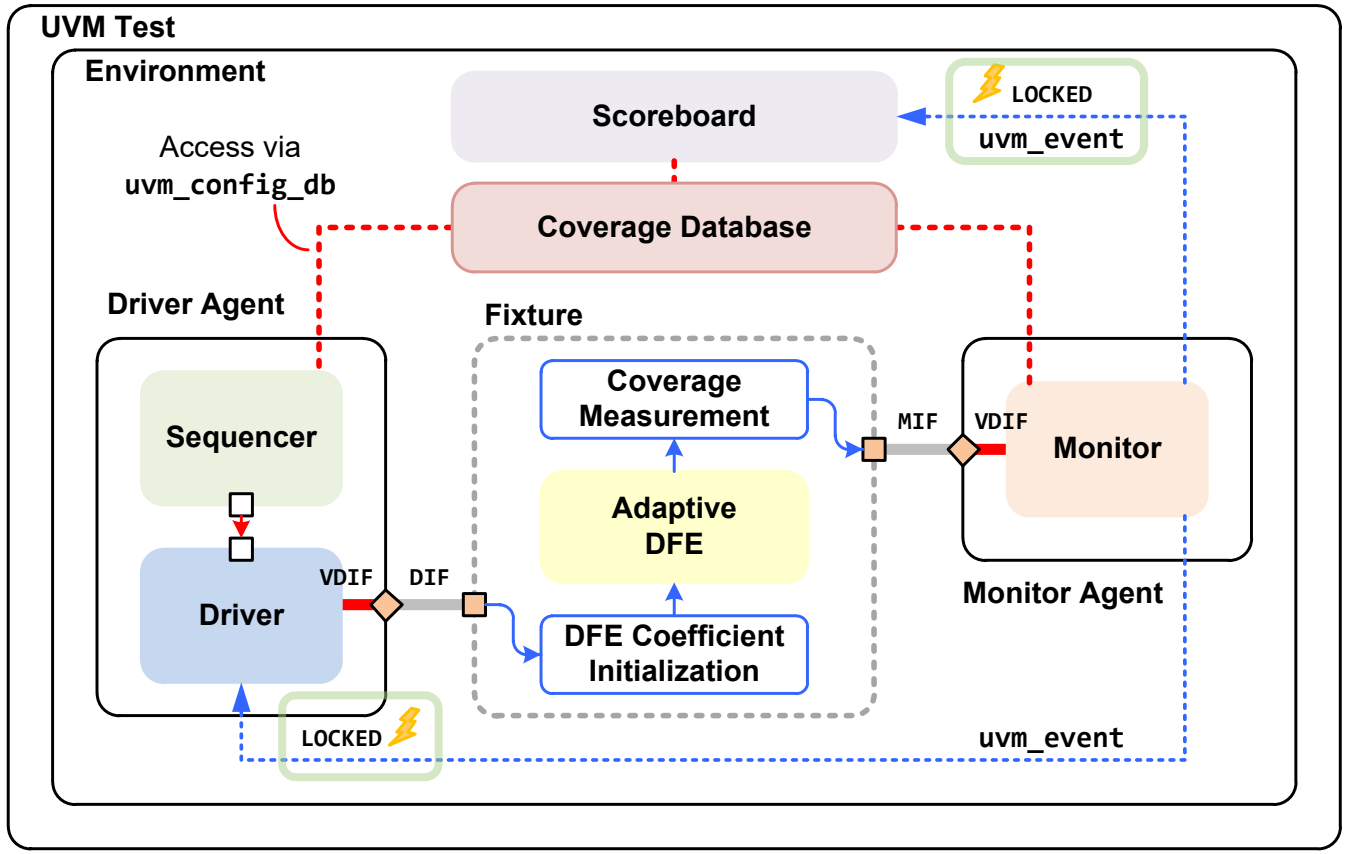
Shared State-Coverage Database

- A ***coverage database*** shared via *uvm_config_db* keeps record of the traversed states and their final states
  - Driver agent consults this database to select the next initial state
  - Monitor agent updates this database with the traversed states once a trial is complete



Global UVM Event

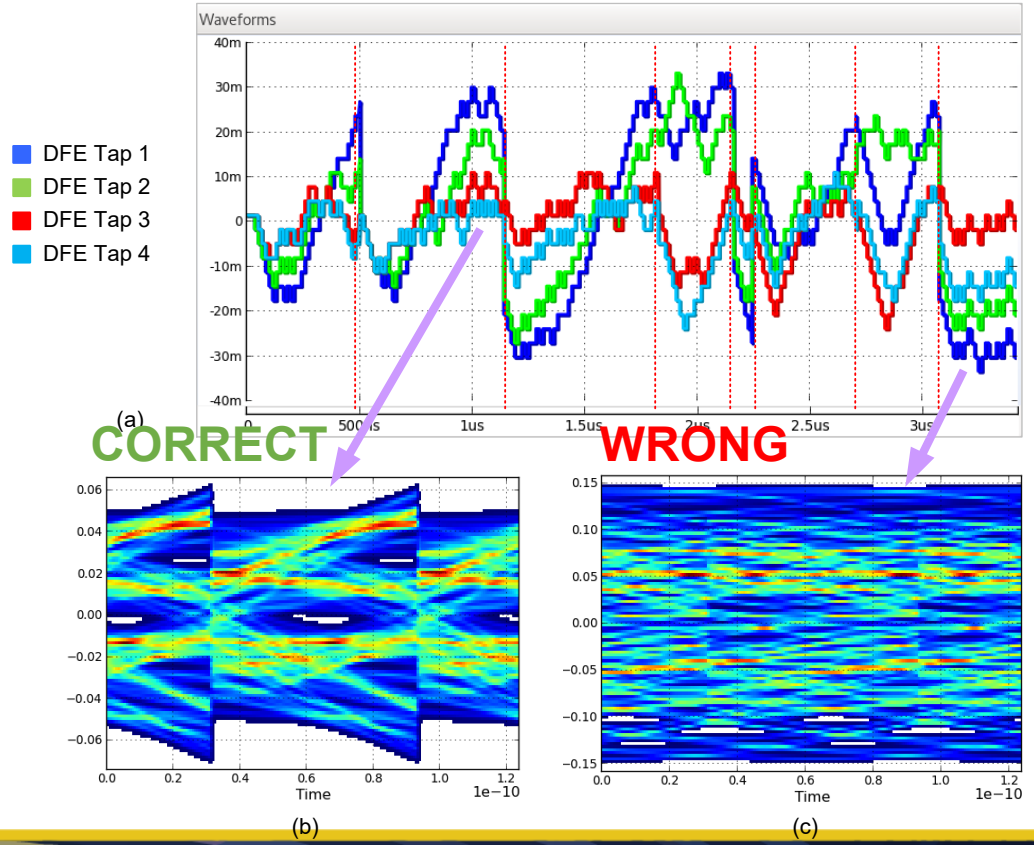
- Monitor triggers a ***global uvm_event*** named *LOCKED* when each trial is complete
  - i.e. when a previously explored state or a new final locked state is reached
  - Driver agent then starts a new trial, until all states have been explored (***PASS***) or more than one final states are found (***FAIL***)
  - Scoreboard reports *PASS/FAIL*



Results with High Channel Loss (-45dB)

- Two different final locked states were found after 7 trials (85 sec. runtime)

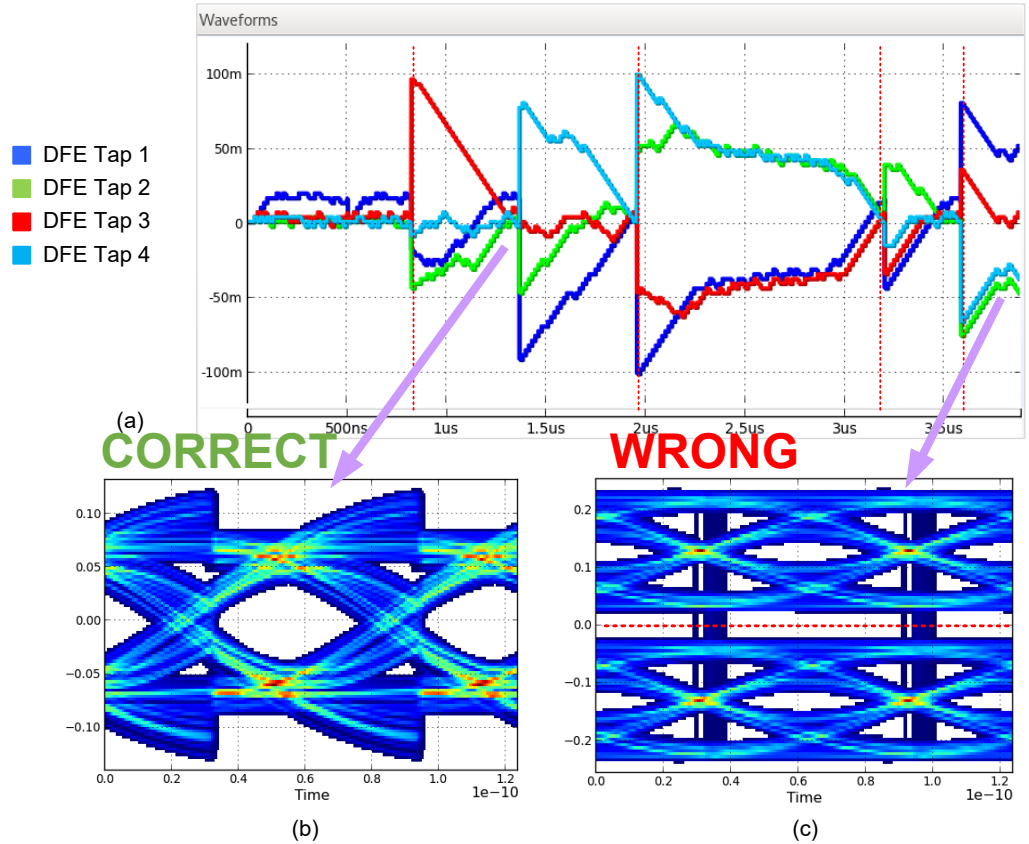
```
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 500.000ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #1: trying new initial state: 10000010000100000100000
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1137.467ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #1: reaching 10011110010010000100000 (final state #1: 10011110010010000100000)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 1138.467ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #2: trying new initial state: 01100101101010000101111O
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1823.684ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #2: reaching 10100110011010001010000 (final state #1: 10011110010010000100000)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 1824.684ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #3: trying new initial state: 10011110010110000001111O
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 2159.451ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #3: reaching 10101010011110001010000 (final state #1: 10011110010010000100000)

  ...

UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 3071.904ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #7: trying new initial state: 01101001110010001001111O
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 3422.325ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #7: reaching 01011101101010000001110O (final state #2: 01011101101010000001110O)

UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(45) @ 3423.325ns: uvm_test_top.E.SCB [SCB]
  | SCB: [FAIL] more than one locked states are found:
    #1: 10011110010010000100000
    #2: 01011101101010000001110O
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(51) @ 3423.325ns: uvm_test_top.E.SCB [SCB]
  | SCB: number of trials = 7, final coverage = 0.999862 (16774909/16777216)
```



Results with Moderate Channel Loss (-20dB)

- -0.1< w_1~w_4< 0.1: two final locked states were found after 6 trials (25 sec.)

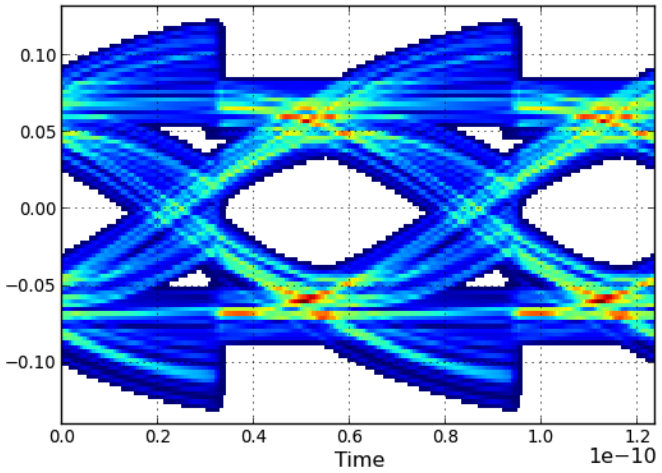
```
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 500.000ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #1: trying new initial state: 10000010000100000100000
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 818.731ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #1: reaching 10011001111110001001111 (final state #1: 10011001111110001001111)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 819.731ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #2: trying new initial state: 01101001001011110011101
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1361.606ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #2: reaching 10011010000100011100000 (final state #1: 10011001111110001001111)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 1362.606ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #3: trying new initial state: 00001101000101111111000
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1952.230ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #3: reaching 10000110000110000110001 (final state #1: 10011001111110001001111)
  ...
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 3580.856ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #6: trying new initial state: 11100100100010101011001011
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 3883.683ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #6: reaching 10111101001010000101010101 (final state #2: 10111101001010000101010101)

UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(45) @ 3884.683ns: uvm_test_top.E.SCB [SCB]
  | SCB: [FAIL] more than one locked states are found:
    #1: 10011001111110001001111
    #2: 10111101001010000101010101
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(51) @ 3884.683ns: uvm_test_top.E.SCB [SCB]
  | SCB: number of trials = 6, final coverage = 1.15037e-05 (193/16777216)
```



Results with Constrained DFE Weights (-20dB Loss)

- Added constraints: $|w_1|+|w_2|+|w_3|+|w_4| \leq 0.05$, $|w_1| > |w_2| > |w_3|$, and $|w_2| > |w_4|$
- Successful global convergence is verified after 1721 trials (5hr 12min)
  - Saved 626 trials out of 2347 (26.7% reduction)

CORRECT




```
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 500.000ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #1: trying new initial state: 10000010000010000100000
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 882.482ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #1: reaching 10010010000010000100001 (final state #1: 10010010000010000100001)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 883.482ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #2: trying new initial state: 01100101101010000101110
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1074.667ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #2: reaching 10001110000110001010000 (final state #1: 10010010000010000100001)
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 1075.667ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #3: trying new initial state: 10011110010001111100000
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 1155.357ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #3: reaching 10011010000110000100001 (final state #1: 10010010000010000100001)
...
UVM_INFO /users/jaeha/projects/UVM_eqadapt/uvm_tb/DRV_PKG.sv(40) @ 83992.481ns: uvm_test_top.E.AGNTD.DRV [DRV]
  | DRV #1721: trying new initial state: 10010101101101111001100
UVM_INFO /users/jaeha/projects/UVM_eqadapt/uvm_tb/MON_PKG.sv(62) @ 84024.354ns: uvm_test_top.E.AGNTM.MON [MON]
  | MON #1721: reaching 10010101101101111001100 (final state #1: 10010010000010000100001)

UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(41) @ 84025.354ns: uvm_test_top.E.SCB [SCB]
  | SCB: [PASS] all tested initial states lead to the same locked state.
UVM_INFO /PATH/UVM_eqadapt/uvm_tb/SCB_PKG.sv(51) @ 84025.354ns: uvm_test_top.E.SCB [SCB]
  | SCB: number of trials = 1721, final coverage = 1.0 (16777216/16777216)
```

Summary

- A UVM testbench that can verify the global convergence property of an analog/mixed-signal system (e.g. adaptive DFE) is demonstrated
  - Checks whether it reaches the same final state regardless of the initial state value
  - Launches a sequence of trial runs to explore all possible initial states of the system
- To support its unique stimulus-response pattern, the testbench uses:
  - A state-coverage database shared via *uvm_config_db*
  - A global *uvm_event* shared via *uvm_event_pool*
- This work was supported by Samsung Electronics, Co. Ltd. and the EDA tools were supported by IDEC and Scientific Analog, Inc.